REMARKS

The Remarks are in response to the Office Communication mailed on March 20, 2007, having a one-month, non-extendable response time. The Communication allowed all of the pending claims (claims 40-54), but required compliance with the provisions of 37 CFR §41.202(a). As noted below for 37 CFR §41.202(a)(1), claims 40-54 are exact copies of claims 1-15 from U.S. patent 6,525,986. It is noted that this information has largely been present previously, prior to the institution of 37 CFR §41.202(a)(1)-(6). An Office Communication mailed on August 17, 2004, also having a one-month non-extendable response period, required the corresponding information as part of a Request for Interference under the earlier rules.

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Section (1) requires sufficient information to identify the patents with which the interference is sought.

Claims 40-54 are exact copies of claims 1-15 from U.S. patent 6,525,986 of Prutchi *et al.* granted February 25, 2003.

(2) Identification of Claims Believed to Interfere, Proposed Count, and Claim Correspondence

Section (2) requires that all claims believed to interfere are identified, that one or more counts is proposed, and that it is shown how the claims correspond to the one or more counts.

Claims 40-54 are exact copies of claims 1-15 from U.S. patent 6,525,986 and, consequently, so correspond. As all of these claims originate from the same patent, it is proposed that these claims could all be taken to correspond to a single count. Although the validity of this grouping has not been considered in detail, to facilitate the Interference process, the following is suggested:

Claim 40 of the present application, which is a copy of claim 1 of U.S. patent number 6,525,986, is suggested as Count 1:

Count 1

> A method comprising:
> receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a

second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;

enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and

disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

Under the grouping suggested above for convenience, claims 40-54 (and claims 1-15 from U.S. patent 6,525,986) would also correspond to Count 1 under the suggested correspondence.

(3) Claim Chart for the Count

As the proposed Count 1 is Claim 40 of the present application, they correspond exactly:

Claim 40 of Present Application	Count 1
40. A method comprising:	A method comprising:
receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;	receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;
enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and	enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and
disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.	disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

The proposed Count 1 is an exact copy of claim 1 of U.S. patent number 6,525,986 and so corresponds:

Claim 1 of U.S. patent number 6,525,986	Count 1
1. A method comprising:	A method comprising:

receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;	receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;
enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and	enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and
disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.	disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

As claim 40 of the present application and claim 1 of U.S. patent number 6,525,986 both correspond to Count 1 and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

As specified in the "Cross-Reference to Related Application" section, as amended by the Preliminary Amendment filed concurrently with the present application, of paragraph [0001] of the application, the present application is a continuation entitled to an effective filing date of July 26, 1991 due to the benefit of:

U.S. Application Serial No. 09/939,290, filed on August 22, 2001, now Patent No. 6,715,044,
U.S. Application Serial No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812,
U.S. Application Serial No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363,
U.S. Application Serial No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070,
U.S. Application Serial No. 08/396,488, filed on March 2, 1995, now abandoned,
U.S. Application Serial No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859.

U.S. patent number 6,525,986 is shown to have a United States filing date of January 22, 2001, claiming priority from a series of continuations and divisions back to U.S. Application Serial No. 08/903,313, filed on July 30, 1997, now Patent No. 5,987,357. The earliest of these U.S. applications is well over six years later than the July 26, 1991, effective filing date of the present application.

(5,6) Claim Charts

The following claim charts show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Device Select Scheme and Circuit" aspect of the present invention. This is primarily described in paragraphs [0016] and [0017] of the Summary and under section entitled "Device Select Scheme and Circuit", found in paragraphs [0062]-[0071], although additional details are provided in other sections. Particular attention is called to paragraphs [0069]-[0071].

References are to the clean version of the Substitute Specification submitted concurrently with the filing of the present application.

40. A method comprising: receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;	Fig. 2A shows a plurality of chips (141), each connected to a pad (149), with an address code set by the connections 161, each of which are distinct. The address is sent to all chips along bus 135. ¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address

	is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."
enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and	¶[0069], lns. 9-11: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected."
disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.	¶[0069], lns. 11-12: "On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."

41. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing two or more bits of the received address with the first programmable code.	¶[0016], lns. 3-14: "Each memory device chip has a multi-bit set of pinouts ..." See Fig. 5A for the connection of these pinouts at 147 being supplied to Comp 305.

42. The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing the portion of the received address with a selection logic circuit.	¶[0069], lns. 7-8: "The comparator 305 [Fig. 5A] compares this address with that obtained from the device-select pinouts 147."

43. The method of claim 40 including comparing the portion of the received address with a first selection logic circuit of the first memory chip and with a second selection logic circuit of the second memory chip.	Each chip 141 has a Device Selection Circuit 203 (details Figs. 4 and 5A. The operation is described beginning at line 1 of paragraph [0069].

44. The method of claim 40 further comprising providing the address to a memory array of each of the plurality of memory chips.	¶[0016], lns. 9-11: "To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus."

45. A method comprising: assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat."
receiving a portion of an address at the first memory chip and at the second memory chip;	¶[0069], lns. 4-12: "a 5-bit array address is shifted into a shift register 311 from the serial-in lines …"
comparing the portion of the address to the first selection code and to the second selection code; and	¶[0069], lns. 7-8: "The comparator 305 [Fig. 5A] compares this address with that obtained from the device-select pinouts 147."
enabling the first memory chip and disabling the second memory chip based on the comparison.	¶[0069], lns. 9-12: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will

	be LOW and the device is not selected."

46. The method of claim 45 further comprising receiving the address at a first memory array of the first memory chip and at a second memory array of the second memory chip.	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."

47. The method of claim 45 wherein assigning includes coupling a bonding pad to a voltage level.	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat." ¶[0049], lns. 2-4: "By selectively grounding certain pads, such as a pad 161 on the mount, each mount may be configured or "keyed" to designate a definite address of the array."

48. The method of claim 45 wherein assigning includes setting a programmable link.	¶[0017]: "The invention provides a simple scheme for assigning an array address to each of the chips mounted on a memory module's backplane..." ¶[0049], lns. 2-4: "By selectively grounding certain pads, such as a pad 161 on

	the mount, each mount may be configured or "keyed" to designate a definite address of the array."

49. The method of claim 45 wherein enabling the first memory chip and disabling the second memory chip based on the comparison includes enabling the first memory chip when the first selection code matches the portion of the address and disabling the second memory chip when the second selection code differs from the portion of the address.	¶[0069], lns. 4-12: ", a 5-bit array address is shifted into a shift register 311 from the serial-in lines SI0 237, SI1 239. The clocking signal is carried in by the control line P/D* 235 which is gate-enabled by a HIGH signal in the master chip select line CS* 171. The 5-bit array address is then passed from the shift register 311 via the bus 313 to the comparator 305. The comparator 305 compares this address with that obtained from the device-select pinouts 147. The comparator output 306 goes HIGH whenever the addresses match. This output is clocked into the address-match register 307 by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 will be LOW and the device is not selected."

50. The method of claim 45 wherein assigning the first selection code to the first memory chip and the second selection code to the second memory chip includes assigning the first selection code to the first memory chip and separately assigning the second	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array

selection code to the second memory chip.	via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."

51. A method comprising: coupling a plurality of address lines of a first memory chip in parallel with a plurality of address lines of a second memory chip;	Fig. 2A shows a plurality of chips (141), each connected to a pad (149), with an address code set by the connections 161, each of which are distinct. The address is sent to all chips along bus 135. The address lines are SI0 and SI1, as shown in Fig. 5A.
setting a first code at the first memory chip;	¶[0064], lns. 3-4: "the address for each location in the array is defined by the grounding configuration or "key" of the mount 149 thereat."
receiving a portion of an address at the first memory chip;	¶[0069], lns. 4-12: "a 5-bit array address is shifted into a shift register 311 from the serial-in lines …"
enabling the first memory chip if the received address portion matches the first code; and	¶[0069], lns. 9-11: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected."
otherwise disabling the first memory chip.	¶[0069], lns. 11-12: "On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."

52. The method of claim 51 wherein enabling the first memory chip includes disabling the second memory chip.	¶[0069], lns. 9-12: "This output is clocked into the address-match register 307 [Fig. 5A] by the falling edge of CS* 171. This results in a S-R register 315 being set HIGH such that DS 309 is also HIGH and the device is selected. On the other hand, when the addresses do not match, DS 309 [Fig. 5A] will be LOW and the device is not selected."

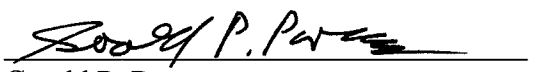
53. The method of claim 51 further including coupling a plurality of data lines of the first memory chip in parallel with a plurality of data lines of the second memory chip.	See Fig. 2A or 2B. The chips 141 are connected in parallel to the bus 135.

54. The method of claim 51 further comprising setting a second code at the second memory chip independent of the first code.	¶[0016], lns. 8-12: "When a memory chip is powered on, the address of the array as defined by the mount key is passed onto the device select circuit of the chip. To select a given memory chip, the correct array address for that chip is sent to all the chips in the array via the interconnecting serial bus. This address is compared at each chip with that it acquired from its each chips mount, and the chip that matched is selected or enabled by its device select circuit."

Conclusion

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and that the requirements of 37 CFR §41.202(a) have been met. A phone call to the undersigned is invited should there be any questions.

Respectfully submitted,



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